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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,991	10/17/2003	Kevin T. Campbell	LSI.83US01 (03-1818)	1384

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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,991	CAMPBELL ET AL.	
	Examiner	Art Unit	
	Don P. Le	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, 5, 8, 10, 14, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Mori (US 4,406,5370).

3. With respect to claim 1, figures 1-10 of Mori teach a method for detecting a page boundary in a data stream comprising:

determining a page size (figure 10, A);

storing said page size in a binary page size register, said binary page register having a predetermined number of bits (figure 10, A);

receiving a data stream address, said data stream address being a binary address corresponding to said data stream (encoder A1, figure 4);

performing a Boolean logic operation on said data stream address and said page size using a Boolean logic gate to produce a binary output value (OUTPUT OF A1, figure 4);

comparing said binary output value with a predetermined binary value using a comparator (A2, figure 4); and

causing a boundary signal to change state when said output value is equal to said predetermined binary value (output of A2, figure 4).

4. With respect to claims 4, 5, 14 and 16, figure 4 of Mori discloses the said Boolean logic operation is an XOR operation (column 6, lines 2).

5. With respect to claims 8 and 17, figure 10 of Mori discloses the resister is a memory device (figure 10, A).

6. With respect to claim 10, figures 1-10 of Mori disclose an apparatus comprising:

a binary page size register (figure 19, A) having a predetermined number of bits that is capable of storing a page size;

an address input (inherent with memory circuit) for receiving a data stream address that is a binary address corresponding to said data stream;

a Boolean logic operator (A2, FIGURE 4) having said binary page size register and said address input as inputs and a resultant output;

a binary compare register (memory) having a predetermined number of bits; and

a comparator (A2, figure 4) that compares said resultant output and said binary compare register and generates a comparator output.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2, 3, 5-7 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (US 4,406,537) in view of Mano (Digital Design, 1984). The apparatus of Mori discloses Boolean Logic operator as an XOR and does not specifically discloses any other logic operators. Mano discloses an XOR with equivalent circuits (figure 4-22) having other logic operators such as AND, NAND, OR and NOR. It would have been obvious to one of ordinary

skill of art at the time the invention was made to have implement the XOR of Mori with equivalent circuit having logic gates AND, NAND, OR and NOR as a design choice as taught by Mano (notice, XOR is equivalent XNOR with inverted input.)

9. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (US 4,406,537). Mori does not specifically disclose the circuit as part of an integrated circuit. It is well known in the art that logic gates and memories can be implemented on an integrated circuit for the purpose of lower cost production and small size in implementation. It would have been obvious to one of ordinary skill of art at the time the invention was made to have implemented the apparatus of Mori in an integrated circuit for the purpose of lower costs and smaller size.

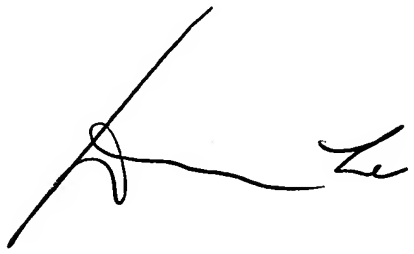
Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

6/6/2005



DON LE
PRIMARY EXAMINER